



ASIC Implementation of High Speed Area Efficient Arithmetic Unit using GDI based Vedic Multiplier

¹M. Sangeetha

²Kishore Balasubramanian

³M. Sowmiya

¹Assistant Professor, Department of Electrical and Electronics Engineering, Dr. Mahalingam College of Engineering and Technology, India

²Assistant Professor, Department of Electrical and Electronics Engineering, Dr. Mahalingam College of Engineering and Technology, India

³Assistant Professor, Department of Electronics and Communication Engineering, PSG Institute of Technology and Applied Research, India



Corresponding author:

M. Sangeetha

sangee.muruganantham@gmail.com

Received: April 21, 2017

Revised: April 28, 2017

Published: April 30, 2017

ABSTRACT

The Concentration of this paper is the designing and implementation of an Arithmetic Logic Unit (ALU) using certain area optimizing techniques such as Vedic Multiplier Algorithm for Multiplication Process & Gate-Diffusion-input (GDI) logic for basic elements. The main sub-blocks of ALU are Adder, Multiplier, Multiplexer and Logical Block. This paper evaluates and compares the performance and optimized area of ALU with CMOS technique and GDI technique in 180nm CMOS process technology. Simulations are performed by using Cadence 180nm technology and compared with CMOS logic realization. The simulation gives that design of ALU through GDI is more efficient with low power consumption, decreases area and faster compared with CMOS logic.

Keywords- ALU, GDI, CMOS, Vedic Multiplier, Optimized ALU.

INTRODUCTION

The performance of Arithmetic Unit mainly depends on speed of the Multiplier. Multiplication is an important fundamental function in arithmetic operations. Multiplication-based operations such as convolution, Fast Fourier Transform (FFT), filtering and Arithmetic Logic Unit (ALU) in microprocessor need its function at the most. In many Digital Signal Processor algorithms multiplication dominates the execution time, so there is a need of high speed multiplier in the ALU. Further it is needed to be operated with lower power to ensure a longer backup time. Thus power reduction is utmost needed for this requirement.

The increased complexity of various applications, demands not only faster multiplier chips but also smarter and efficient multiplying algorithms that can be implemented in the chips. Two most common multiplication algorithms followed in the digital hardware are array multiplication and booth multiplication algorithms. The drawback of these two algorithms is a large propagation delay associated with it.

GATE DIFFUSION INPUT (GDI) LOGIC

Gate Diffusion Input (GDI Cell) method is based on the use of a simple cell. At a basic cell reminds the standard CMOS inverter, but there are some important differences:

1. Gate Diffusion Input (GDI CELL) contains three inputs

- a) G (common gate input of NMOS and PMOS)
- b) P (input to the source/drain of PMOS)
- c) N (input to the source/drain of NMOS).

2. Both NMOS and PMOS bulks are connected to N or P, so it can be arbitrarily biased at contrast with CMOS inverter. It must be remarked, that not all the functions are possible in standard P-Well CMOS process, but can be successfully implemented in Twin-Well CMOS. The change in input configuration of the Gate Diffusion Input (GDI) CELL corresponds to six different Boolean functions.

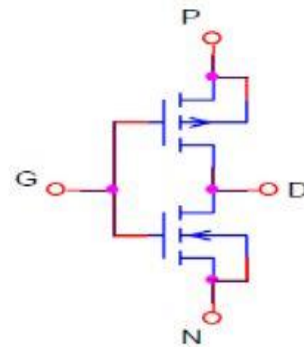


Fig-1: Basic structure of GDI cell

Table-1: Functions of GDI Logic

N	P	G	Function
B	0	A	AB
1	B	A	A+B
C	B	A	A'B+AC
0	1	A	A'
0	B	A	A'B
B	1	A	A'+B

Most of these functions are intricate (6-12 transistors) in CMOS, as well as in standard CMOS implementations, but in GDI only 2 transistors per function were used. Gate

Diffusion Input (GDI CELL) structure is different from the subsisting CMOS techniques and has some consequential features, which sanctions ameliorations in design intricacy level, transistor counts, static power dissipation and logic level swing.

COMPARISON OF CMOS 4:1 MUX AND GDI 4:1 MUX

The fig-2 shows the CMOS based 4:1 MUX that having 24T and it provide the power dissipation of 12mw

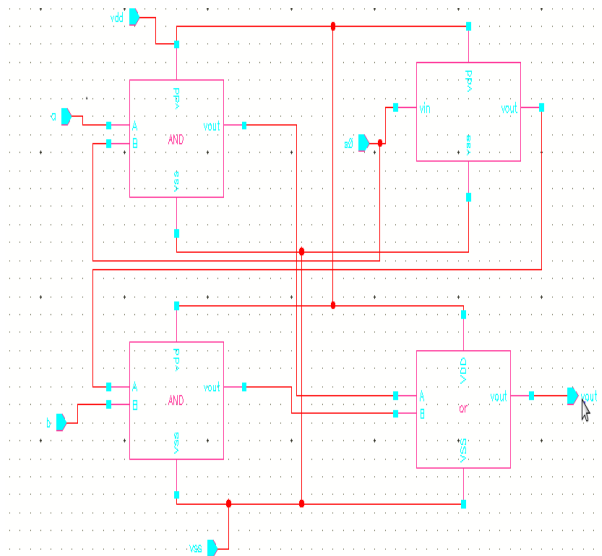


Fig-2: CMOS based Multiplexer

The fig-3 shows the GDI based 4:1 MUX that having 6T and it provide the power dissipation 6.133uw

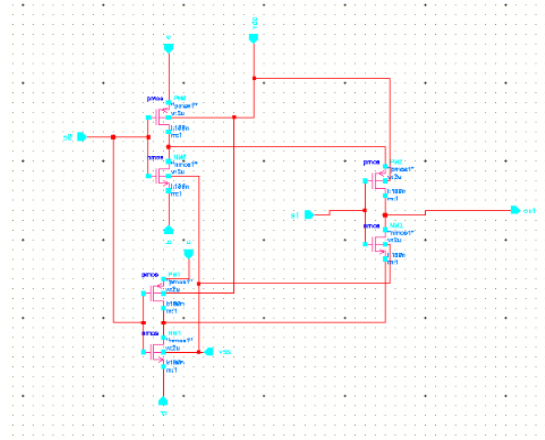


Fig-3: GDI based Multiplexer

COMPARISON OF CMOS AND GDI FULL ADDER

The fig-4 shows the CMOS based Full adder that having 28T and it provide the power dissipation 7.008mw

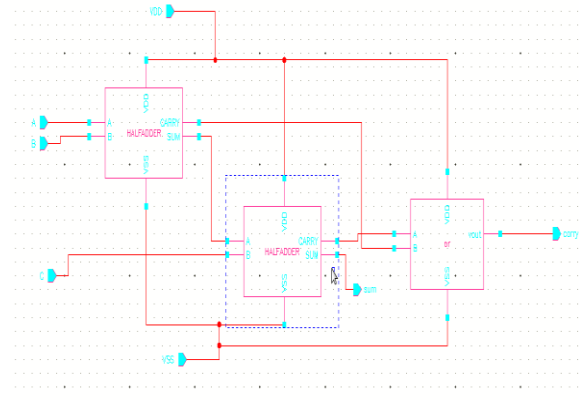


Fig-4: CMOS based Full adder

The Fig-5 shows the GDI based Full adder that having 10T and it provide the power dissipation 6.94nw

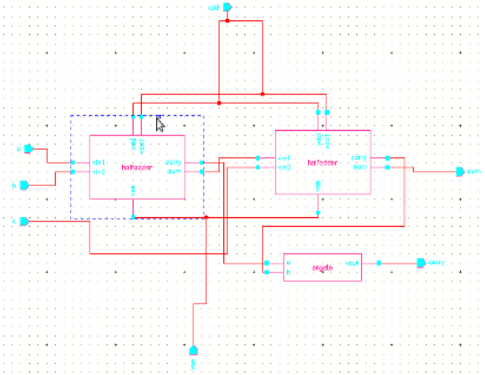


Fig-5: GDI based Full adder

COMPARISON OF CMOS AND GDI 4 BIT REGISTER

The CMOS based 4 bit register using SR Flip-flop is shown in the fig-6 and it provide the power dissipation 12.43mw

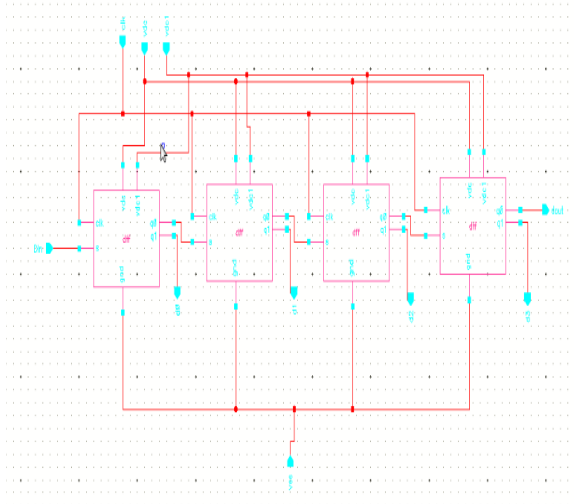


Fig-6: CMOS - 4 Bit Register

The fig-7 shows the GDI based 4 bit register and it provide the power dissipation 49.89uw

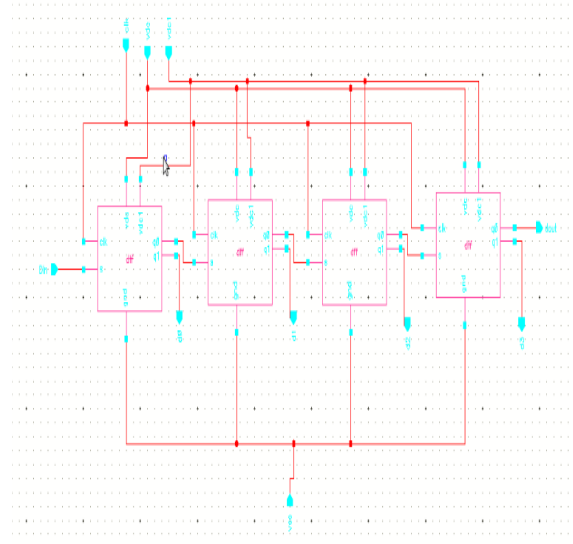


Fig-7: GDI - 4 Bit Register

COMPARISON OF CMOS AND GDI 4X4 VEDIC MULTIPLIER

The CMOS based 4x4 vedic multiplier is shown in the fig-8 and it provide the power dissipation of 110mw.

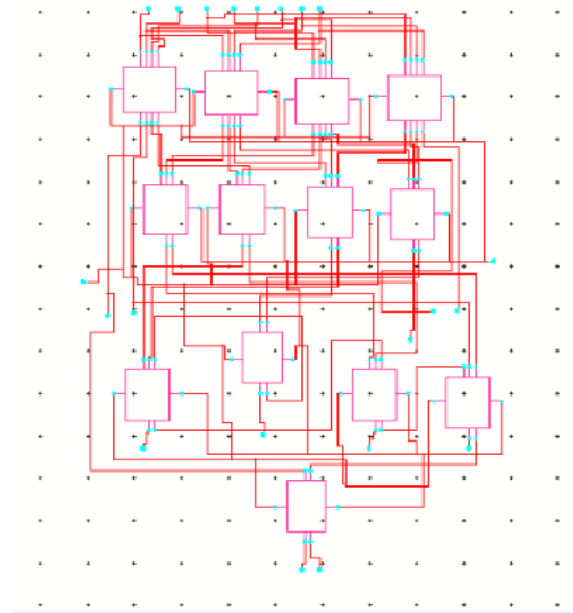


Fig-8: CMOS – 4x4 Vedic Multiplier

The fig-9 shows the GDI based 4x4 Vedic multiplier and it provide the power dissipation of 99nw

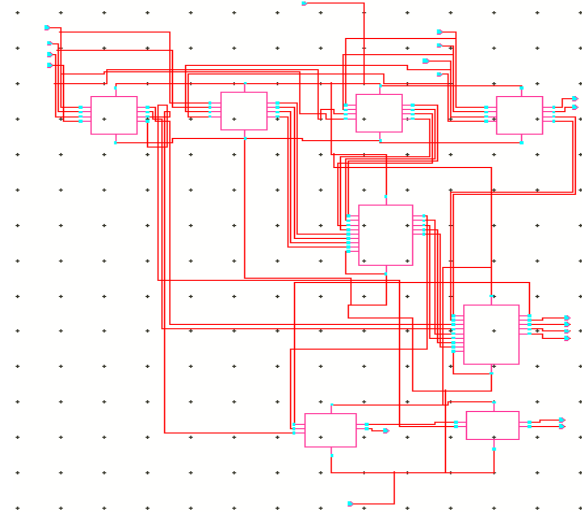


Fig-9: GDI – 4x4 Vedic Multiplier

GDI BASED ALU

The proposed AU shown in Figure 10 accepts two n-bit operands A and B. The input operands are split into $A[N-1:N/2]$ & $A[N/2-1:0]$ and $B[N-1:N/2]$ & $B[N/2-1:0]$. The input multiplexers directed by control inputs S3 - S0 sends the input sub-operands to the respective $n/2 \times n/2$ multiplier units to produce intermediate products which are then compressed by the adder stages to produce final product. In addition the proposed AU performs addition, subtraction and accumulation operations on the inputs. Note that for send back to adder stages.

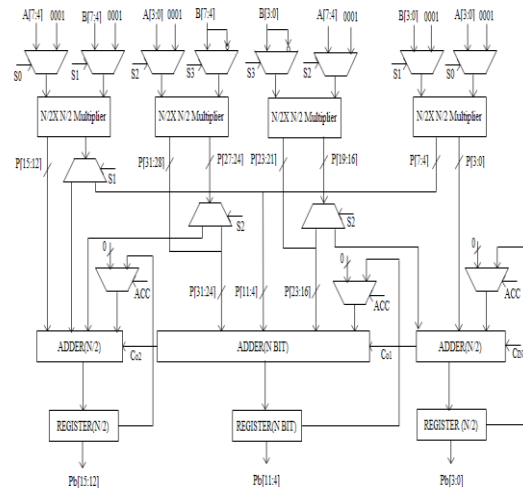


Fig-10: Proposed Arithmetic Unit
a) Addition/ Subtraction

In case of addition operation, the multiplier on the left performs $A[3:0] \times 1$, second one performs $B[3:0] \times 1$, third multiplier performs $B[7:4] \times 1$ while the rightmost multiplier perform $A[7:4] \times 1$. The de-multiplexer controlled through S2 directs the PPs to the next stage adder to compute the result of $A + B$. Note that for subtraction operation, the multiplier on the left performs $A[3:0] \times 1$, while the right multiplier performs $A[7:4] \times 1$ whereas the second and third multiplier performs the complement of $B[3:0] \times 1$ and $B[7:4] \times 1$. The de-multiplexer controlled through S1 and S2 directs the PPs to the next stage adder to compute the result of $A-B$. Also note that for subtract operations (see Fig 2) signal CIN is set to 1, thus enabling 2s complement addition on inputs to realise subtract operation without additional hardware.

b) Multiplication and Accumulation

Multiply–Accumulate operation is a common step that computes the product of

two numbers and adds the product to accumulator. To perform accumulation operation, the results of the addition are sent back to the data path through multiplexers controlled by signal ACC in the proposed AU.

SIMULATIONS RESULTS AND ANALYSIS

Simulations were performed in 180nm CMOS technology, with a supply voltage of 5 V. The schematic entry is done in CADENCE VIRTUOSO and verifications are done using CADENCE ASSURA. When compared to base Vedic ALU design the proposed ALU Design will be better. The simulated output of 4x1 multiplexer, Full Adder and 4x4 Vedic Multiplier is shown in the Figures. The number of transistor required and power consumption for the individual cells of the ALU is listed in table II.

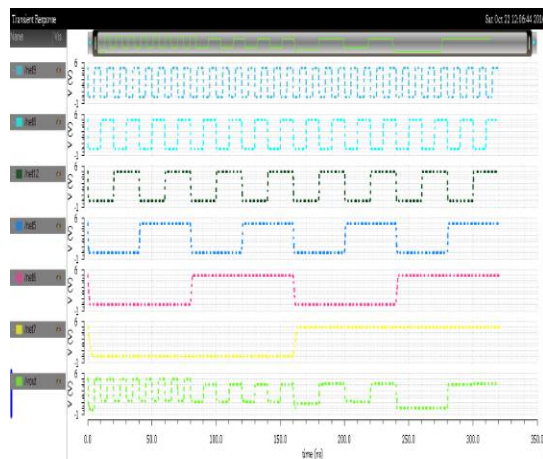


Fig-11: Simulated waveform of Multiplexer

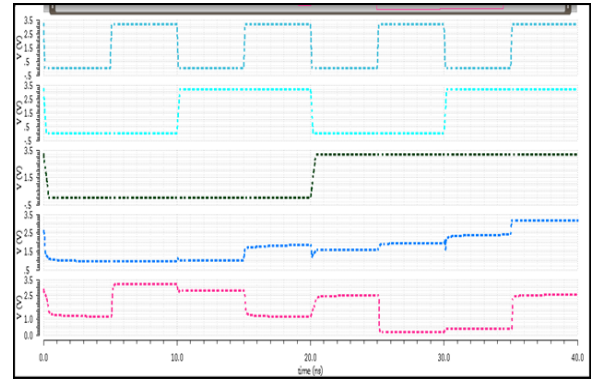


Fig-12: Simulated waveform of Adder

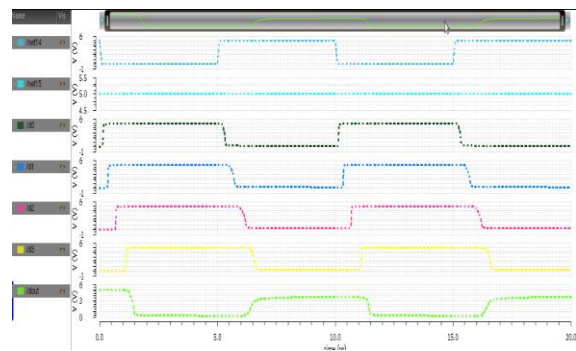


Fig-13: Simulated waveform of 4 bit Register

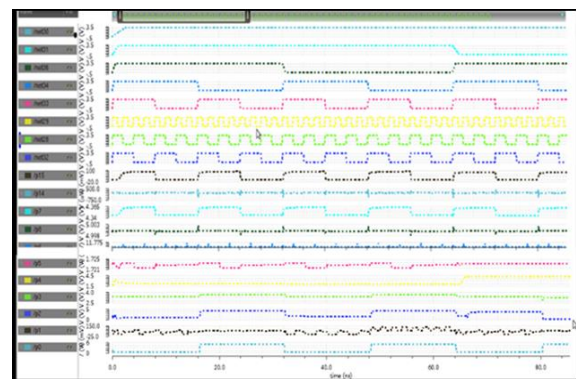


Fig-14: Simulated waveform of 4x4 Vedic Multiplier

TABLE-2: ANALYSIS RESULT OF DIFFERENT BLOCKS OF ALU

Design	Cell	Power	Delay
CMOS	4:1 Mux	12.43mw	18ns
	Full Adder	7.008mw	10.56ns
	4bit Register	12.43mw	18.08ns

	4x4 Vedic Multiplier	110mw	11.45ns
GDI	4:1 Mux	6.1uw	418.9ps
	Full Adder	6.94nw	1.363ns
	4bit Register	49.89um	1.363ns
	4x4 Vedic Multiplier	99nw	11.02ns

CONCLUSION

In this paper, a novel architecture for Arithmetic unit (AU) have been proposed using the concept of Vedic Algorithms and enhanced by eliminating input multiplexers. The proposed architecture using the Urdhva Triyagbhyam sutra has resulted in reduced delay and power consumption which intern provides high speed and energy efficient design due to the parallelism in partial products generation and their summation obtained using the sutra. The basic logic functions inside the AU are designed using GDI logic. From the delay and power, the proposed system viz adder, mux, multiplier, register perform better when compared to existing system. This will increase the speed of AU. This suggests the suitability of proposed AU and it enhanced counterpart for high speed portable applications.

REFERENCES

Khader Mohammad, SosAgaian and Fred Hudson (2010) "Implementation of Digital Electronic Arithmetics and its Application in Image Processing", Computers and Electrical Engineering, 36(3): 424-434.

ManoranjanPradhan, Rutuparna Panda and Sushanta Kumar Sahu (2011) "MAC Implementation using Vedic Multiplication

Algorithm", International Journal of Computer Applications, 21(7): 26-28.

Harish Kumar and A.R. Hemanth Kumar (2015) "Design and Implementation of Vedic Multiplier using Compressors", International Journal of Engineering Research & Technology, 4(6): 230-233.

Virendra B. Magar (2013) "Intelligent and Superior Vedic Multiplier for FPGA Based Arithmetic Circuits", International Journal of Soft Computing and Engineering, 3(3): 31-36.

S.S. Purohit, S.R. Chalamalasetti, M. Margala and W.A. Vanderbauwhede (2013) "Design and Evaluation of High-Performance Processing Elements for Reconfigurable Systems", IEEE Transactions on Very Large Scale Integration (VLSI) Systems 21(10): 1915-1927.

S. Leonard Gibson Moses and M. Thilagar (2010) "VLSI Implementation of High Speed DSP algorithms using Vedic Mathematics", Singaporean Journal Scientific Research, 3(1): 138-140.

Nishant G. Deshpande and RashmiMahajan (2014) "Ancient Indian Vedic Mathematics based 32-Bit Multiplier Design for High Speed and Low Power Processors", International Journal of Computer Applications, 95(24): 19-22.

Irshad Khan, Sunil Shah and Vinod Kapse (2015) "Quick Review on Multiplication Algorithm for Enhancing Efficiency of MAC Unit", Proceedings of International Conference of Advance Research and Innovation, pp. 159-162.